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Analysis, Design, and Implementation of a Zero-Voltage-Transition Interleaved Boost Converter

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Abstract

This study proposes a novel zero voltage transition (ZVT) pulse width modulation (PWM) DC–DC interleaved boost converter with an active snubber cell. All the semiconductor devices in the converter turn on and off with soft switching to reduce the switching power losses and improve the overall efficiency. Through the interleaved approach, the current stresses of the main devices and the ripple of the output voltage and input current are reduced. The main switches turn on with ZVT and turn off with zero voltage switching (ZVS). The auxiliary switch turns on with zero current switching (ZCS) and turns off with ZVS. In addition, the snubber cell does not create additional current or voltage stress on the main switches and main diodes. The proposed converter can smoothly achieve soft switching characteristics even under light load conditions. The theoretical analysis and operating stages of the proposed converter are made for the D > 50% and D < 50% modes. Finally, a prototype of the proposed converter is implemented, and the experimental results are given in detail for 500 W and 50 kHz. The overall efficiency of the proposed converter reached 95.5% at nominal output power.

Key words: Hard switching, Interleaved boost converter, Pulse width modulation, Soft switching, Zero voltage transition

I. INTRODUCTION

DC–DC boost converters are commonly preferred in industrial applications. They are used when the output voltage in renewable energy applications requires boosting because solar cells and fuel cells supply low output voltage [1], [2]. In recent years, interleaved boost converters, which are constructed by connecting classical boost converters in parallel, are chosen for high-power applications. Interleaved boost converters can provide better performance than classic boost converters. They have many advantages, such as the low ripple of input current and output voltage, fast transient response, low input filter sizes, and low current stresses on semiconductor devices for the same power conditions as classic boost converters [3]-[5].

Other important utilization areas of interleaved boost converters include power factor correction (PFC) and photovoltaic (PV) applications. Steady current from the input source is ideal for the improved performance of PFC applications [6], [7]. Similarly, the ripples of input currents at maximum power point tracking lead to additional power losses [8]. Therefore, interleaved boost converters are more suitable than classic boost converters in PFC and PV applications because the ripple of the input current is reduced by the interleaved structure.

Power density should be increased to achieve improved efficiency by reducing the volume and weight of classic and interleaved boost converters. In this case, increasing the switching frequency to a higher power density is required. However, high switching frequency leads to high switching power losses, which are the reverse recovery losses for diodes and electromagnetic interference (EMI) noises. Therefore, it results in poor performance and low efficiency [9]-[11]. To resolve these drawbacks, soft switching (SS) techniques are improved, and soft switching interleaved boost converters have been proposed in the existing literature [12]-[29].

In the converters proposed in [12]-[14], soft switching is achieved for semiconductor devices. The main switches are turned on and off with soft switching. However, two auxiliary switches are used to provide soft switching in these converters. This case results in increased cost and conduction losses. To overcome this problem, some soft switching interleaved boost converters have been proposed in [15]-[18]. In these approaches, the interleaved structure has one

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auxiliary switch. Therefore, their cost and conduction losses are reduced. However, the main switches turn off with hard switching (HS) even though the main switches and the other semiconductor devices turn on with soft switching. Therefore, the switching power losses cannot be set to zero in these approaches. To address this drawback, some converters have been proposed in [19]-[24]. In these approaches, the problems mentioned above are not encountered, and the main switches can be turned on and off with soft switching techniques. In the approaches in [19], [20], the snubber cell operates with soft switching for the main switches, but it results in additional current and voltage stresses on the main switches. Therefore, the conduction losses of the switches increase, and switches with high current/voltage capabilities must be used for converters. Furthermore, only an additional voltage stress occurs on the main switches in the approach in [21]. These problems can be eliminated using the approaches proposed in [22]-[24]. In [22], [23], the main switches and other devices turn on and off with soft switching techniques and without additional current or voltage stresses. However, the resonance inductors of the snubber cell are on the path of the main current. Therefore, the cost and weight of the converter is increased because the inductor size must be increased by considering the main current. Moreover, ringing oscillations occur between the resonance inductors and the parasitic capacitors of the main switches. In addition, this problem causes EMI noises. In the approach of [24] that addresses these problems, the main switches and diodes turn on and off with soft switching techniques. In addition, the snubber cell of the proposed converter has a simple structure and does not cause additional current or voltage stresses on the main devices. However, additional switching power losses occur because the auxiliary switch and diode turn on and off with hard switching.

In this study, a novel zero voltage transition-pulse width modulation (ZVT-PWM) DC–DC interleaved boost converter is proposed. It provides most of the desirable features of interleaved soft switching converters in the literature and overcomes most of their drawbacks. In the proposed converter, the main switches turn on with ZVT and turn off with zero voltage switching (ZVS). In addition, the main diodes turn on with ZVS and turn off with zero current switching (ZCS) without additional current or voltage stresses on the main devices. Furthermore, the auxiliary diodes operate with soft switching, and the auxiliary switch turns on with ZCS and turns off with ZVS. The proposed interleaved converter has a simple and low-cost structure. All of the semiconductor devices excellently turn on and off with soft switching techniques in a wide load ranges. The proposed converter eliminates the switching power losses that occur in the classic interleaved boost converter. Therefore, it can be conveniently used in high-power and renewable energy applications, such as fuel cells, solar cells, PFC, PV, and battery charging.

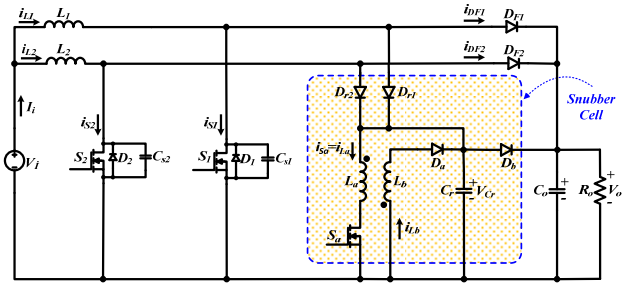


Fig. 1. Basic circuit of the proposed ZVT-PWM DC–DC interleaved boost converter.

The basic circuit of the proposed ZVT-PWM DC–DC interleaved boost converter is shown in Fig. 1. In addition, we have presented this novel snubber cell in a conference using simulation results. The conference paper is provided in ref. [30]. In addition, we have extended and improved our conference paper. This paper presents our conference paper's extended version with mathematical analysis, experimental results, efficiency analysis, and detailed presentation of other features.

II. Operating Modes of the Proposed Converter

In the basic circuit scheme of the converter shown in Fig. 1, V_i is the input voltage source, S_1 and S_2 are the main switches, D_1 and D_2 are the body diodes of the main switches, L_1 and L_2 are the main inductors, D_{F1} and D_{F2} are the main diodes, C_o is the output filter capacitor, and C_{S1} and C_{S2} are the sums of the parasitic capacitors of the main switches and the other parasitic capacitors. In the snubber cell, S_a is the auxiliary switch, L_a and L_b are the coupled resonance inductors, C_r is the resonance capacitor, and D_{r1}, D_{r2}, D_a, and D_b are the auxiliary diodes.

The proposed interleaved converter has two operating modes: D > 50% and D < 50%. The following assumptions are made to facilitate the theoretical analysis of the two modes.

- The input voltage V_i is constant.
- C_o is assumed large enough such that the output voltage can be kept constant.
- L_1 and L_2 are assumed large enough to keep the input current constant. Their values are equal, and the sum of their currents is equal to the input current.
- L_a and L_b are coupled inductors, and their values are equal. In addition, their values are significantly smaller than the main inductors.
- All semiconductor devices are assumed ideal.
- The reverse recoveries of the diodes are ignored.

A. Operating Stages of D > 50% Mode

In this mode, the steady state operation of the converter has

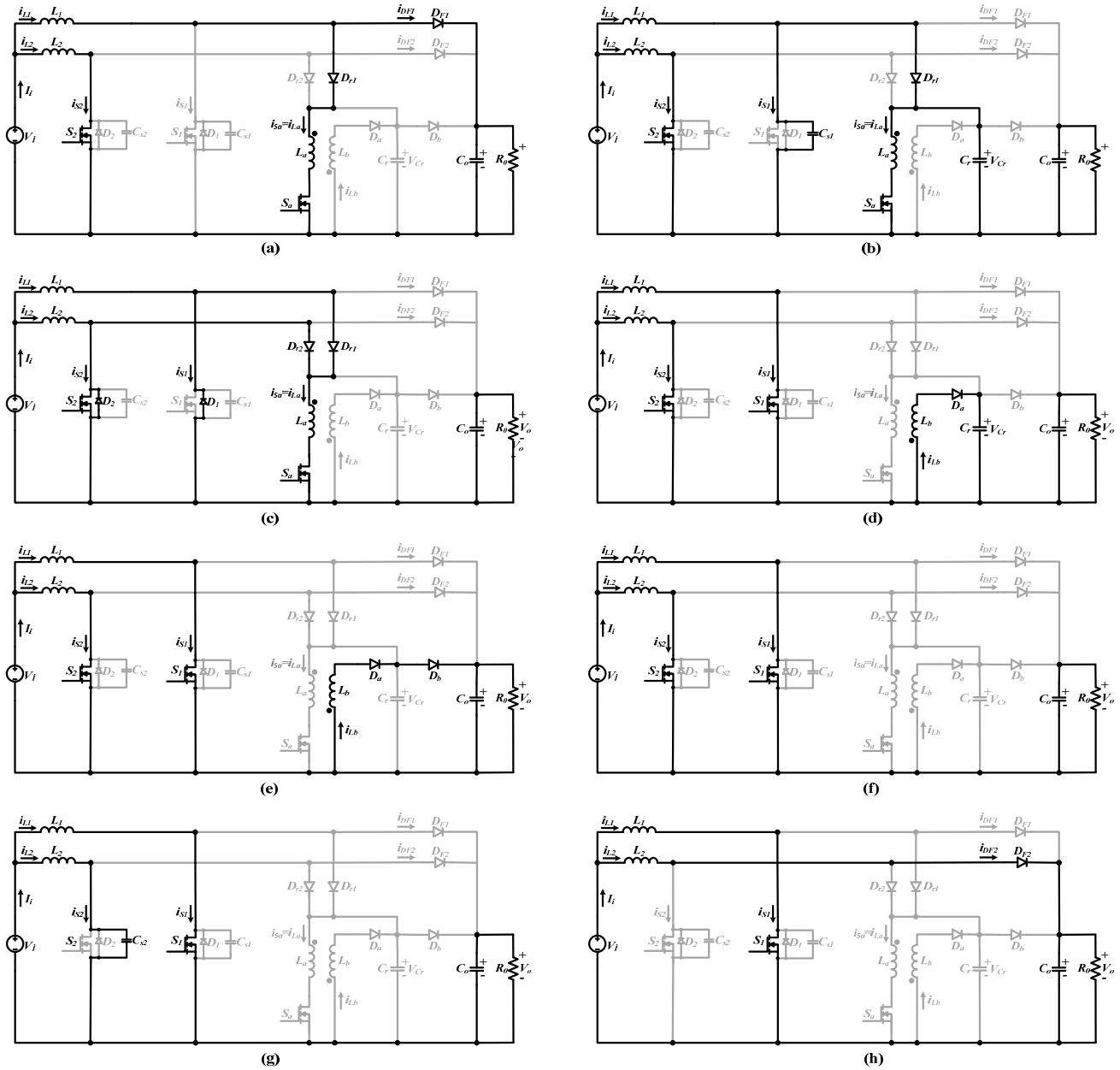


Fig. 2. Equivalent circuits of the operating stages for the D > 50% mode in the proposed ZVT-PWM DC–DC interleaved boost converter; (a) $t_0 < t < t_1$, (b) $t_1 < t < t_2$, (c) $t_2 < t < t_3$, (d) $t_3 < t < t_4$, (e) $t_4 < t < t_5$, (f) $t_5 < t < t_6$, (g) $t_6 < t < t_7$, (h) $t_7 < t < t_8$.

16 stages in one switching cycle. Here, only the eight stages for switch S_1 are analyzed because the operating principle of the interleaved structure is symmetrical. The key waveforms of the operation stages of the D > 50% mode are shown in Fig. 3.

Stage 1 [$t_0 < t < t_1$: Fig. 2(a)]

At the start of this stage, the main switch S_2 is at the on state, and the other switches are at the off state. The current of L_2 flows through the main switch S_2, and the current of L_1 flows through the main diode D_{F1}. At $t = t_0$, $i_{S1} = 0$, $i_{S2} = I_{L2}$, $i_{Sa} = i_{La} = i_{Lb} = 0$, $i_{DF1} = I_{L1}$, $i_{DF2} = 0$, and $v_{Cr} = V_o$ are valid. When a control signal is applied to the auxiliary switch S_a, the current of auxiliary switch i_{Sa} increases, and the current of main diode i_{DF1} decreases simultaneously. Therefore, S_a turns on and D_{F1} turns off with ZCS because of the L_a inductor connected in series. The resonance inductor current $i_{La}(t)$ and the resonance capacitor voltage v_{Cr} (t) can be expressed as follows:

$$i_{La}(t) = \frac{V_o}{L_a} \cdot (t - t_0) \tag{1}$$

$$v_{Cr}(t) = V_o \tag{2}$$

During this stage,

$$t_{01} = \frac{L_a \cdot I_{L1}}{V_o} \tag{3}$$

is derived. At $t = t_1$, this stage ends as soon as i_{DF1} equals zero and i_{Sa} reaches I_{L1}.

Stage 2 [$t_1 < t < t_2$: Fig. 2(b)]

At t = t_1, $i_{S1} = 0$, $i_{S2} = I_{L2}$, $i_{Sa} = i_{La} = I_{L1}$, $i_{Lb} = 0$, $i_{DF1} = 0$, $i_{DF2} = 0$, and $v_{Cr} = V_o$ are valid. In this stage, two parallel resonances occur through $C_{s1} - D_{r1} - L_a - S_a$ and $C_r - L_a - S_a$. Therefore, capacitors C_r and C_{s1} discharge while the current of L_a continues to increase in sinusoidal form. The resonant inductor current i_{La} (t) and the resonant capacitor voltage v_{Cr} (t) can be expressed as follows:

$$i_{La}(t) = I_{L1} + \frac{V_o}{Z_1} \cdot \sin \omega_1 (t - t_1) \tag{4}$$

$$v_{Cr}(t) = v_{Cs1}(t) = V_o \cdot \cos \omega_1 (t - t_1) \tag{5}$$

During this stage,

$$t_{12} = \frac{\pi}{2 \cdot \omega_1} = \frac{\pi}{2} \sqrt{L_a \cdot (C_{S1} + C_r)} \tag{6}$$

is derived. In these equations,

$$Z_1 = \sqrt{\frac{L_a}{C_{S1} + C_r}} \tag{7}$$

$$\omega_1 = \frac{1}{\sqrt{L_a \cdot (C_{S1} + C_r)}} \tag{8}$$

are valid. At t = t_2, this stage ends when the voltages of C_r and C_{S1} reach zero. At the end of this stage, the current of L_a will reach its maximum value (I_{La2}).

Stage 3 [$t_2 < t < t_3$: Fig. 2(c)]

During this stage, $i_{S1} = (I_{L1} - I_{La2}/2)$, $i_{S2} = (I_{L2} - I_{La2}/2)$, $i_{Sa} = i_{La} = I_{La2}$, $i_{Lb} = 0$, $i_{DF1} = 0$, $i_{DF2} = 0$, and $v_{Cr} = 0$ are valid. The excess of I_{La2} from the input current flows through internal diodes D_1 and D_2 of the main switches. This stage is a freewheeling interval called a ZVT interval. At any time during this interval, a control signal is applied to the main switch S_1, and the control signal of auxiliary switch S_a is removed simultaneously. Therefore, the main switch S_1 turns on with ZVT, and the auxiliary switch S_a turns off with ZVS. Here, the on-duration of auxiliary switch t_{03} must be more than $t_{01} + t_{12}$ to achieve turning on with ZVT. The following equations are provided for this stage:

$$t_{03} \geq t_{01} + t_{12} = \frac{L_a \cdot I_{L1}}{V_o} + \frac{\pi}{2} \sqrt{L_a \cdot (C_{S1} + C_r)} \tag{9}$$

$$i_{La}(t) = I_{La2} \tag{10}$$

$$v_{Cr}(t) = 0 \tag{11}$$

Stage 4 [$t_3 < t < t_4$: Fig. 2(d)]

At t = t_3, $i_{S1} = I_{L1}$, $i_{S2} = I_{L2}$, $i_{Sa} = i_{La} = 0$, $i_{Lb} = I_{La2}$, $i_{DF1} = 0$, $i_{DF2} = 0$, and $v_{Cr} = 0$ are valid. Through coupling, the energy of L_a is transferred to L_b when the auxiliary switch is turned off. Thereafter, resonance between L_b and C_r is achieved. During this stage, some parts of the energy of resonant inductor L_b is transferred to resonant capacitor C_r. Auxiliary switch S_a turns off with ZVS because of this resonance. The following equations are provided For this stage:

$$i_{Lb}(t) = I_{La2} \cdot \cos \omega_2 (t - t_3) \tag{12}$$

$$v_{Cr}(t) = I_{La2} \cdot Z_2 \cdot \sin \omega_2 (t - t_3) \tag{13}$$

During this stage,

$$t_{34} = \frac{\pi}{2 \cdot \omega_2} = \frac{\pi}{2} \sqrt{L_b \cdot C_r} \tag{14}$$

is derived. In these equations,

$$Z_2 = \sqrt{\frac{L_b}{C_r}} \tag{15}$$

$$\omega_2 = \frac{1}{\sqrt{L_b \cdot C_r}} \tag{16}$$

are valid. At t = t_4, this stage ends when v_{Cr} reaches V_o and D_b diode turns on with ZVS. In addition, the current of L_b decreases to a valid value (I_{Lb4}).

Stage 5 [$t_4 < t < t_5$: Fig. 2(e)]

At t = t_4, $i_{S1} = I_{L1}$, $i_{S2} = I_{L2}$, $i_{Sa} = i_{La} = 0$, $i_{Lb} = I_{Lb4}$, $i_{DF1} = i_{DF2} = 0$, and $v_{Cr} = V_o$ are valid. This stage begins when diode D_b turns on with ZVS. Thereafter, the remaining energy of L_b is transferred to the output through diodes D_a and D_b. The following equations are provided for this stage:

$$i_{Lb}(t) = I_{Lb4} - \frac{V_o}{L_b} \cdot (t - t_4) \tag{17}$$

$$v_{Cr}(t) = V_o \tag{18}$$

During this stage,

$$t_{45} = \frac{I_{Lb4}}{V_o} \cdot L_b \tag{19}$$

is derived. At t = t_5, when the current of L_b reaches zero, diodes D_a and D_b turn off with ZCS, and this stage ends.

Stage 6 [$t_5 < t < t_6$: Fig. 2(f)]

During this stage, $i_{S1} = I_{L1}$, $i_{S2} = I_{L2}$, $i_{Sa} = i_{La} = i_{Lb} = 0$, $i_{DF1} = i_{DF2} = 0$, and $v_{Cr} = V_o$ are valid. Main switches S_1 and S_2 are at the on state, and auxiliary switch S_a is at the off state. The energy obtained from the input voltage source is transferred to main inductors L_1 and L_2. In this stage, the snubber cell is passive, and the main switches conduct the input current ($i_{S1} + i_{S2} = I_i$). At t = t_6, the control signal of main switch S_2 is removed, and this stage ends.

Stage 7 [$t_6 < t < t_7$: Fig. 2(g)]

At t = t_6, $i_{S1} = I_{L1}$, $i_{S2} = I_{L2}$, $i_{Sa} = i_{La} = i_{Lb} = 0$, $i_{DF1} = i_{DF2} = 0$, and $v_{Cr} = V_o$ are valid. In this stage, main switch S_1 conducts the current of L_1, and capacitor C_{S2} is charged linearly by the current of L_2. The following equations are written for this stage:

$$v_{Cs2}(t) = \frac{I_{L2}}{C_{S2}} \cdot (t - t_6) \tag{20}$$

During this stage,

$$t_{67} = \frac{V_o}{I_{L2}} \cdot C_{S2} \tag{21}$$

is derived. At t = t_7, this stage ends after the voltage of C_{s2} reaches the output voltage. Therefore, main diode D_{F2} turns on with ZVS.

Stage 8 [$t_7 < t < t_8$: Fig. 2(h)]

During this stage, $i_{S1} = I_{L1}$, $i_{S2} = 0$, $i_{Sa} = i_{La} = i_{Lb} = 0$, $i_{DF1} =$

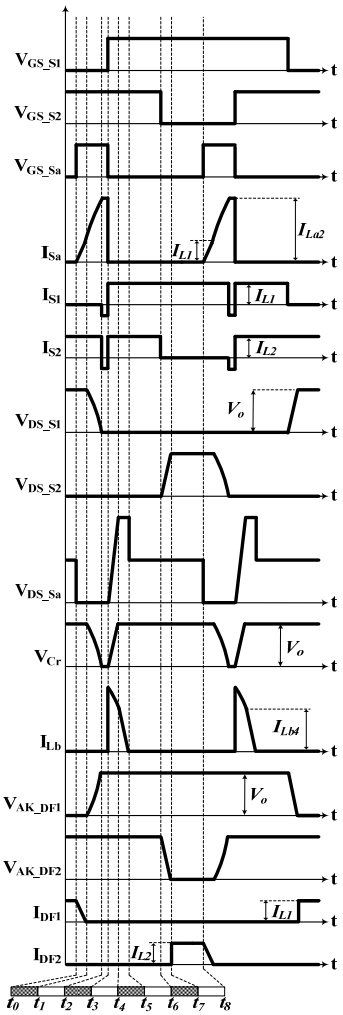


Fig. 3. Key waveforms of the operation stages of the proposed ZVT-PWM DC–DC interleaved boost converter for the D > 50% mode.

0, $i_{DF2} = I_{L2}$, and $v_{Cr} = V_o$ are valid. In addition, main switch S_1 is at the on state, and S_2 is at the off state. At $t = t_8$, a control signal is applied to auxiliary switch S_a, and this stage is completed. Therefore, a half switching cycle is completed for switch S_1. In the next period, the same stages continue periodically for switch S_2.

B. Operating Stages of D < 50% Mode

In this mode, the steady state operation of the converter has 16 stages in one switching cycle. In this section, only the eight stages of S_1 are analyzed because the interleaved structure is symmetrical. Fig. 4 shows the equivalent circuits for the D < 50% mode. The key waveforms of the operation stages of the D < 50% mode are shown in Fig. 5.

Stage 1 [$t_0 < t < t_1$: Fig. 4(a)]

At the start of this stage, all switches are at the off state. The input current flows through main diodes D_{F1} and D_{F2}. At $t = t_0$, $i_{S1} = 0$, $i_{S2} = 0$, $i_{Sa} = i_{La} = i_{Lb} = 0$, $i_{DF1} = I_{L1}$, $i_{DF2} = I_{L2}$, and $v_{Cr} = V_o$ are valid. When a control signal is applied to auxiliary switch S_a, the current of the auxiliary switch increases and the currents of the main diodes decrease simultaneously. Therefore, S_a turns on and the main diodes turn off with ZCS because of the L_a inductor connected in series. Resonance inductor current i_{La} (t) and resonance capacitor voltage v_{Cr} (t) can be expressed as follows:

$$i_{La}(t) = \frac{V_o}{L_a} \cdot (t - t_0) \tag{22}$$

$$v_{Cr}(t) = V_o \tag{23}$$

During this stage,

$$t_{01} = \frac{L_a \cdot I_i}{V_o} \tag{24}$$

is derived. At $t = t_1$, i_{Sa} reaches I_i when i_{DF1} and i_{DF2} decrease to zero. Therefore, this stage ends.

Stage 2 [$t_1 < t < t_2$: Fig. 4(b)]

At $t = t_1$, $i_{S1} = 0$, $i_{S2} = 0$, $i_{Sa} = i_{La} = I_i$, $i_{Lb} = 0$, $i_{DF1} = 0$, $i_{DF2} = 0$, and $v_{Cr} = V_o$ are valid. In this stage, three parallel resonances occur through $C_{s1} – D_{r1} – L_a – S_a$, $C_{s2} – D_{r2} – L_a – S_a$, and $C_r – L_a – S_a$. Therefore, capacitors C_r, C_{s1}, and C_{s2} discharge while the current of L_a continues to increase in sinusoidal form. Resonant inductor current i_{La} (t) and resonant capacitor voltage v_{Cr} (t) can be expressed as follows:

$$i_{La}(t) = I_i + \frac{V_o}{Z_3} \cdot \sin \omega_3 (t - t_1) \tag{25}$$

$$v_{Cr}(t) = v_{Cs1}(t) = v_{Cs2}(t) = V_o \cdot \cos \omega_3 (t - t_1) \tag{26}$$

During this stage,

$$t_{12} = \frac{\pi}{2 \cdot \omega_3} = \frac{\pi}{2} \sqrt{L_a \cdot (C_{S1} + C_{S2} + C_r)} \tag{27}$$

is derived. In these equations,

$$Z_3 = \sqrt{\frac{L_a}{C_{S1} + C_{S2} + C_r}} \tag{28}$$

$$\omega_3 = \frac{1}{\sqrt{L_a \cdot (C_{S1} + C_{S2} + C_r)}} \tag{29}$$

are valid. At $t = t_2$, this stage ends when the voltages of C_r, C_{S1}, and C_{S2} decrease to zero, during which the current of L_a reaches its maximum value (I_{La2}).

Stage 3 [$t_2 < t < t_3$: Fig. 4(c)]

During this stage, $i_{S1} = (I_{L1} - I_{La2} / 2)$, $i_{S2} = (I_{L2} - I_{La2} / 2)$, $i_{Sa} = i_{La} = I_{La2}$, $i_{Lb} = 0$, $i_{DF1} = 0$, $i_{DF2} = 0$, and $v_{Cr} = 0$ are valid. The current over the input current of I_{La2} flows through internal diodes D_1 and D_2 of the main switches. This stage is a freewheeling interval called ZVT. At any time during this interval, a control signal is applied to main switch S_1, and the control signal of auxiliary switch S_a is removed simultaneously. Therefore, main switch S_1 turns on with ZVT, and auxiliary switch S_a turns off with ZVS. Here, the on-duration of auxiliary switch t_{03} must be greater than $t_{01} + t_{12}$ to achieve turning on with ZVT. For this stage, the following equations are written:

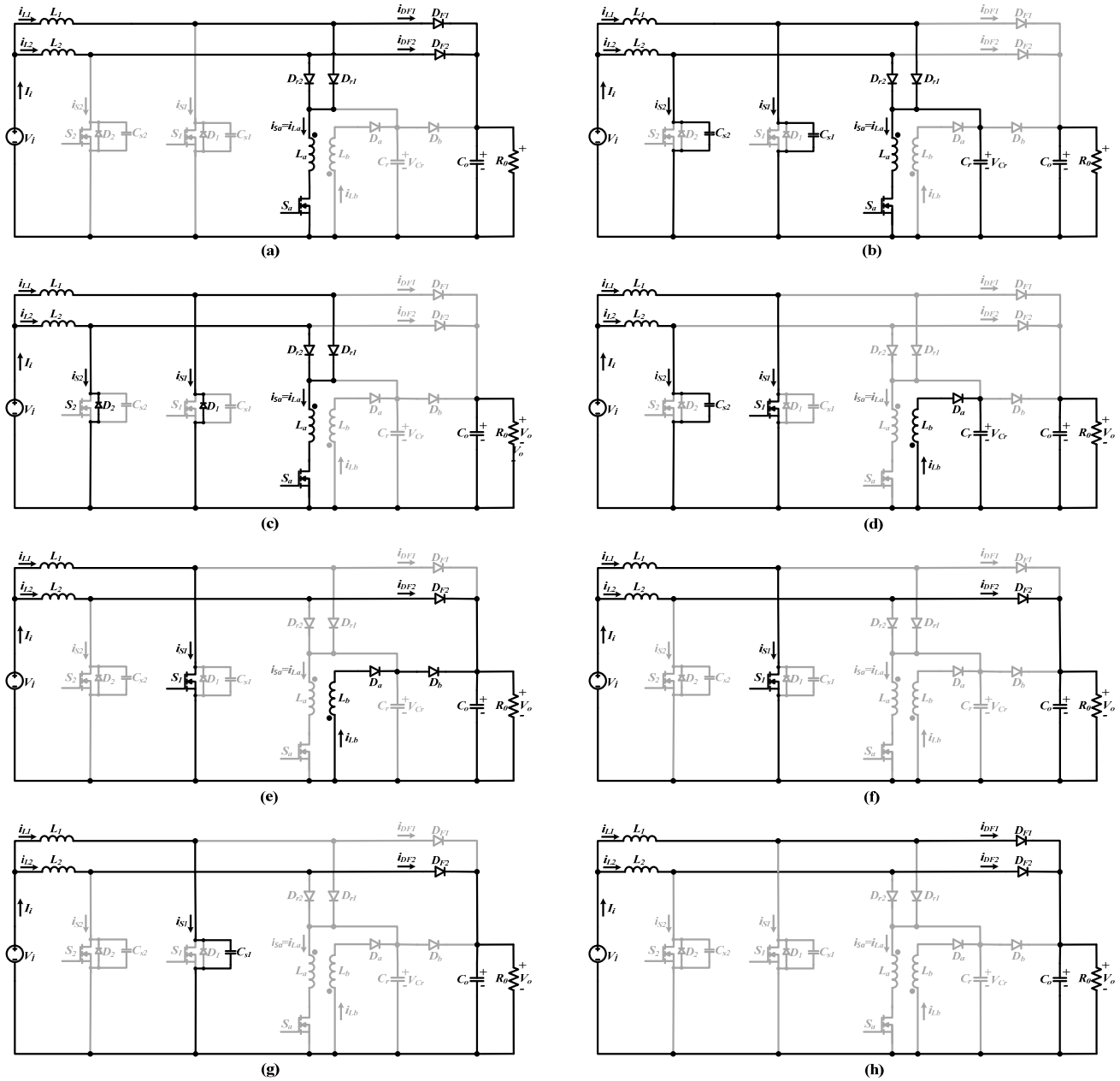


Fig. 4. Equivalent circuit of the operating stages for the D < 50% mode in the proposed ZVT-PWM DC–DC interleaved boost converter; (a) $t_0 < t < t_1$, (b) $t_1 < t < t_2$, (c) $t_2 < t < t_3$, (d) $t_3 < t < t_4$, (e) $t_4 < t < t_5$, (f) $t_5 < t < t_6$, (g) $t_6 < t < t_7$, (h) $t_7 < t < t_8$.

$$t_{03} \geq t_{01} + t_{12} = \frac{L_a \cdot I_i}{V_o} + \frac{\pi}{2}\sqrt{L_a \cdot (C_{S1} + C_{S2} + C_r)} \tag{30}$$

$$i_{La}(t) = I_{La2} \tag{31}$$

$$v_{Cr}(t) = 0 \tag{32}$$

Stage 4 [$t_3 < t < t_4$: Fig. 4(d)]

At $t = t_3$, $i_{S1} = I_{L1}$, $i_{S2} = 0$, $i_{Sa} = i_{La} = 0$, $i_{Lb} = I_{La2}$, $i_{DF1} = 0$, $i_{DF2} = 0$, and $v_{Cr} = 0$ are valid. In this stage, main switch S_1 conducts the current of L_1, and capacitor C_{S2} is linearly charged by the current of L_2. In addition, the energy of L_a is transferred to L_b when the auxiliary switch is turned off. Thereafter, resonance occurs between L_b and C_r. During this stage, some parts of the energy of resonant inductor L_b is transferred to resonant capacitor C_r. Auxiliary switch S_a turns off with ZVS because of this resonance. The following equations are provided for this stage:

$$i_{Lb}(t) = I_{La2} \cdot \cos\omega_4 (t - t_3) \tag{33}$$

$$v_{Cr}(t) = I_{La2} \cdot Z_4 \cdot \sin\omega_4 (t - t_3) \tag{34}$$

$$v_{Cs2}(t) = \frac{I_{L2}}{C_{s2}} \cdot (t - t_3) \tag{35}$$

During this stage,

$$t_{34} = \frac{\pi}{2 \cdot \omega_4} = \frac{\pi}{2}\sqrt{L_b \cdot C_r} \tag{36}$$

is derived. In these equations,

$$Z_4 = \sqrt{\frac{L_b}{C_r}} \tag{37}$$

$$\omega_4 = \frac{1}{\sqrt{L_b \cdot C_r}} \tag{38}$$

are valid. At t = t_4, when the voltages of C_{s2} and C_r reach V_o, main diode D_{F2} and diode D_b turn on with ZVS. Therefore, this stage ends. The current of the L_b inductor decreases to a valid value of I_{Lb4} at the end of this stage.

Stage 5 [$t_4 < t < t_5$: Fig. 4(e)]

At t = t_4, $i_{S1} = I_{L1}$, $i_{S2} = 0$, $i_{Sa} = i_{La} = 0$, $i_{Lb} = I_{Lb4}$, $i_{DF1} = 0$, $i_{DF2} = I_{L2}$, and $v_{Cr} = V_o$ are valid. This stage begins when diode D_b turns on with ZVS. Thereafter, the remaining energy of L_b is transferred to the output through diodes D_a and D_b. For this stage, the following equations are provided:

$$i_{Lb}(t) = I_{Lb4} - \frac{V_o}{L_b} \cdot (t - t_4) \tag{39}$$

$$v_{Cr}(t) = V_o \tag{40}$$

During this stage,

$$t_{45} = \frac{I_{Lb4}}{V_o} \cdot L_b \tag{41}$$

is derived. At t = t_5, when the current of L_b decreases to zero, diodes D_a and D_b turn off with ZCS, and this stage ends.

Stage 6 [$t_5 < t < t_6$: Fig. 4(f)]

During this stage, $i_{S1} = I_{L1}$, $i_{S2} = 0$, $i_{Sa} = i_{La} = i_{Lb} = 0$, $i_{DF1} = 0$, $i_{DF2} = I_{L2}$, and $v_{Cr} = V_o$ are valid. Main switch S_1 is at the on state, main switch S_2 is at the off state, and auxiliary switch S_a is at the off state. This stage is a freewheeling interval where the snubber cell is inactive.

At t = t_6, the control signal of main switch S_1 is removed, and this stage ends.

Stage 7 [$t_6 < t < t_7$: Fig. 4(g)]

At t = t_6, $i_{S1} = I_{L1}$, $i_{S2} = 0$, $i_{Sa} = i_{La} = i_{Lb} = 0$, $i_{DF1} = 0$, $i_{DF2} = I_{L2}$, and $v_{Cr} = V_o$ are valid. In this stage, capacitor C_{S1} is linearly charged by the current of L_1 after the control signal of S_1 is removed. For this stage, the following equations are given:

$$v_{Cs1}(t) = \frac{I_{L1}}{C_{S1}} \cdot (t - t_6) \tag{42}$$

During this stage,

$$t_{67} = \frac{V_o}{I_{L1}} \cdot C_{S1} \tag{43}$$

is derived. At t = t_7, this stage ends immediately after the voltage of C_{s1} reaches the output voltage. Therefore, main diode D_{F1} turns on with ZVS.

Stage 8 [$t_7 < t < t_8$: Fig. 4(h)]

During this stage, $i_{S1} = 0$, $i_{S2} = 0$, $i_{Sa} = i_{La} = i_{Lb} = 0$, $i_{DF1} = I_{L1}$, $i_{DF2} = I_{L2}$, and $v_{Cr} = V_o$ are valid. In addition, main switches S_1 and S_2 are at the off state, and main diodes D_{F1} and D_{F2} conduct the input current. At t = t_8, a control signal is applied to auxiliary switch S_a, and this stage is completed.

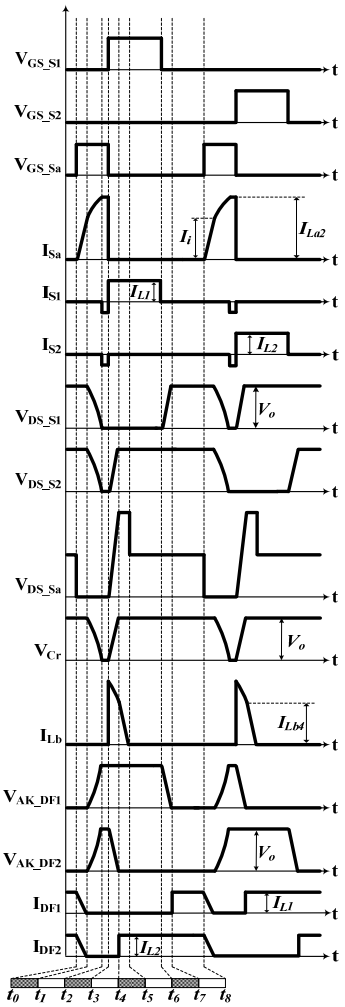


Fig. 5. Key waveforms of the operation stages of the proposed ZVT-PWM DC–DC interleaved boost converter for the D < 50% mode.

Therefore, a half switching cycle is completed for switch S_1. In the next period, the same stages continue periodically for switch S_2.

C. Voltage Ratios of the D > 50% and D < 50% Modes

In the proposed converter, the input and output voltage ratios are not the same in the D > 50% and D < 50% modes. Therefore, the equations of the voltage ratios for the two modes must be derived. Fig. 6 shows the control signals of the switches and the waveforms of the boost inductor currents for the real and simplified durations in the D > 50% mode. If some transient stages are ignored, then the current of boost inductor L_1 is as provided in the following equations while main switch S_1 is at the on and off states. Table I shows the correspondence between the real stages and the simplified ones in the D > 50% mode.

$$\sum_{S1=on} \Delta i_{L1} = \frac{V_i \cdot (\Delta t_{ba} + \Delta t_{fb})}{L_1} = \frac{V_i \cdot (D_{S1} + D_{Sa}) \cdot T}{L_1} \tag{44}$$

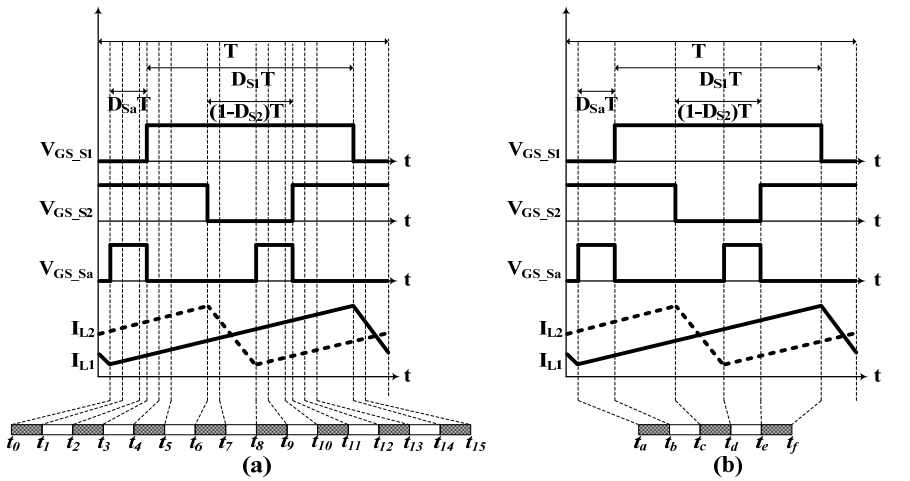


Fig. 6. Control signals of the switches and the waveforms of the boost inductor currents in the D > 50% mode for (a) real durations and (b) simplified durations.

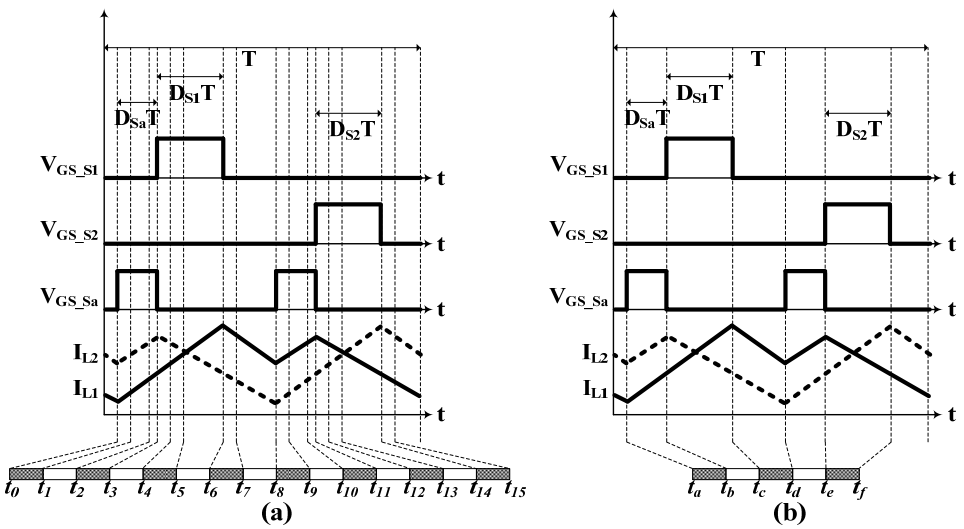


Fig. 7. Control signals of the switches and the waveforms of the boost inductor currents in the D < 50% mode for (a) real durations and (b) simplified durations.

TABLE I
CORRESPONDENCE BETWEEN THE REAL DURATIONS AND THE SIMPLIFIED DURATIONS (D > 50%)

Real Operating Durations	Simplified Operating Durations
$[t_0\text{-}t_3]$	$[t_a\text{-}t_b] = \Delta t_{ba}$
$[t_3\text{-}t_{14}]$	$[t_b\text{-}t_f] = \Delta t_{fb}$
$[t_{14}\text{-}t_0]$	$[t_f\text{-}t_a] = [T_p - t_{af}] = \Delta t_{af}$

$$\sum_{S1=off} \Delta i_{L1} = \frac{(V_o - V_i)\cdot \Delta t_{af}}{L_1} = \frac{(V_o - V_i)\cdot \left[1-(D_{S1}+D_{Sa})\cdot T\right]}{L_1} \quad (45)$$

Therefore, the input and output voltage ratio can be derived from Eqs. (44) and (45) a:

$$\frac{V_o}{V_i} = \frac{1}{1-(D_{S1}+D_{Sa})} \quad (46)$$

TABLE II
CORRESPONDS BETWEEN THE REAL DURATIONS AND THE SIMPLIFIED DURATIONS (D < 50%)

Real Operating Durations	Simplified Operating Durations
$[t_0\text{-}t_3]$	$[t_a\text{-}t_b] = \Delta t_{ba}$
$[t_3\text{-}t_6]$	$[t_b\text{-}t_c] = \Delta t_{cb}$
$[t_6\text{-}t_8]$	$[t_c\text{-}t_d] = \Delta t_{dc}$
$[t_8\text{-}t_{11}]$	$[t_d\text{-}t_e] = \Delta t_{ed}$
$[t_{11}\text{-}t_{14}]$	$[t_e\text{-}t_f] = \Delta t_{fe}$
$[t_{14}\text{-}t_0]$	$[t_f\text{-}t_a] = [T_p - t_{af}] = \Delta t_{af}$

Similarly, Fig. 7 shows the control signals of the switches and the waveforms of the boost inductor currents for the real and simplified durations in the D < 50% mode. In this manner, if some transient stages are ignored, then the current of boost inductor L_1 is as provided in the following equations while

TABLE III
PARAMETERS OF THE EXPERIMENTAL CIRCUIT

Parameter	Symbol	Value
Duty cycle	*D*	*D > 50%* *D < 50%*
Output capacitor	C_o	*470 μF*
Boost inductors	L_1, L_2	*1 mH*
Resonance inductor	L_a, L_b	*12 μH*
Resonance capacitor	C_r	*3.3 nF*
Parasitic capacitors	C_{s1}, C_{s2}	*1 nF*

main switch S_1 is at the on and off states. Table II shows the correspondence between the real stages and the simplified ones in the D > 50% mode.

$$\sum_{S1=on} \Delta i_{L1} = \frac{V_i \cdot (\Delta t_{ba} + \Delta t_{cb} + \Delta t_{ed})}{L_1} = \frac{V_i \cdot (D_{S1} + 2 \cdot D_{Sa}) \cdot T}{L_1} \quad (47)$$

$$\sum_{S1=off} \Delta i_{L1} = \frac{(V_o - V_i) \cdot (\Delta t_{dc} + \Delta t_{fe} + \Delta t_{af})}{L_1} = \frac{(V_o - V_i) \cdot [1 - (D_{S1} + 2 \cdot D_{Sa}) \cdot T]}{L_1} \quad (48)$$

Therefore, the input and output voltage ratio can be derived from Eqs. (47) and (48) as

$$\frac{V_o}{V_i} = \frac{1}{1 - (D_{S1} + 2 \cdot D_{Sa})} \quad (49)$$

III. DESIGN PROCEDURE

In this section, the design considerations of the proposed converter are presented. The experimental circuit parameters of the proposed converter are given in Table III.

The following assumptions are made to determine the experimental circuit parameters of the proposed converter in the design procedure.

- Output power : $P_o = 500\ W$
- Switching frequency: $f_s = 50\ kHz$
- Input voltage: $V_i = 100–250\ V$
- Output voltage: $V_o = 400\ V$
- Desired efficiency: $\eta > 94\%$
- Ripple of the boost inductors : $\Delta I_{L1}\% = \Delta I_{L2}\% = 30\%$

1) The output capacitor must be sufficiently high to keep the output voltage constant. Therefore, its value is 470 μF.

2) The design procedure of boost inductors L_1 and L_2 can be found in [24]. It should be operated in CCM for both D > 50% and D < 50% modes. Therefore, the minimum value of boost inductor L_1 in D > 50% is

$$L_{1\min} = L_{2\min} = L_{\min}$$
$$L_{\min} = \frac{(D_{S1} + D_{Sa}) \cdot [1 - (D_{S1} + D_{Sa})]^2 \cdot V_o}{I_o \cdot f_s} = 300\mu H \quad (50)$$

The minimum value of boost inductor L_1 in D < 50% is

$$L_{1\min} = L_{2\min} = L_{\min}$$
$$L_{\min} = \frac{(D_{S1} + 2 \cdot D_{Sa}) \cdot [1 - (D_{S1} + 2 \cdot D_{Sa})]^2 \cdot V_o}{I_o \cdot f_s} = 937.5\mu H \quad (51)$$

Therefore, the values of the boost inductors are set to 1 mH.

3) Table I defines the input power P_i and the maximum value of the boost inductor currents I_{Lmax} for a ripple of 30%.

$$\eta = \frac{P_0}{P_i} \geq 0.94 \quad (52)$$

$$P_i \leq 531.91\ \text{W} \quad (53)$$

$$I_{L1\max} = I_{L2\max} = I_{L\max} = 1.15 \cdot \frac{P_i}{2 \cdot V_i} = 3.06\ \text{A} \quad (54)$$

4) The snubber inductor can be selected to ensure the following condition with reference to [25] and [26]. Its current can be equal to the maximum value of the boost inductor current at most within three times the reverse recovery time of the main diode. Here, t_{rr} is the reverse recovery time of the main diode and is provided in Table II. Resonance inductor L_a is determined to minimize the reverse recovery of the main diode from Eq. (54) and Table II as follows:

$$L_a = L_b \geq \frac{V_o \cdot 3 \cdot t_{rr}}{I_{L\max}} \geq 9.8\ \mu\text{H} \quad (55)$$

Therefore, the values of coupled inductors L_a and L_b are set to 12 μH.

5) We assume that the current of the auxiliary switch can be as high as $3I_{Lmax}$. In addition, the following equations can be written from Stages 2 and 7 of the D > 50% mode. In Eq. (57), t_f is the falling time of the main switch and is provided in Table 2. t_f should be less than t_{67} to provide ZVS at turning off.

$$C_{s1} + C_r = \frac{L_a \cdot (I_{Lapk} - I_{L\max})^2}{{V_o}^2} \quad (56)$$

$$t_{67} = \frac{V_o \cdot C_{s2}}{I_{L\max}} \geq t_f \quad (57)$$

Therefore, the values of capacitors C_{s1} and C_{s2} are set to 1 nF, and C_r is set to 3.3 nF using Eqs. (56) and (57) and Table II. The experimental circuit parameters of the proposed converter are provided in Table I.

IV. CONVERTER FEATURES

The proposed ZVT-PWM DC–DC interleaved boost converter has many advantages. It provides the most desirable features of interleaved soft switching converters in the literature and overcomes most of their drawbacks. The features of this novel converter can be summarized briefly as follows:

1) The main switches turn on with ZVT and turn off with ZVS.

2) The auxiliary switch turns on with ZCS because of the

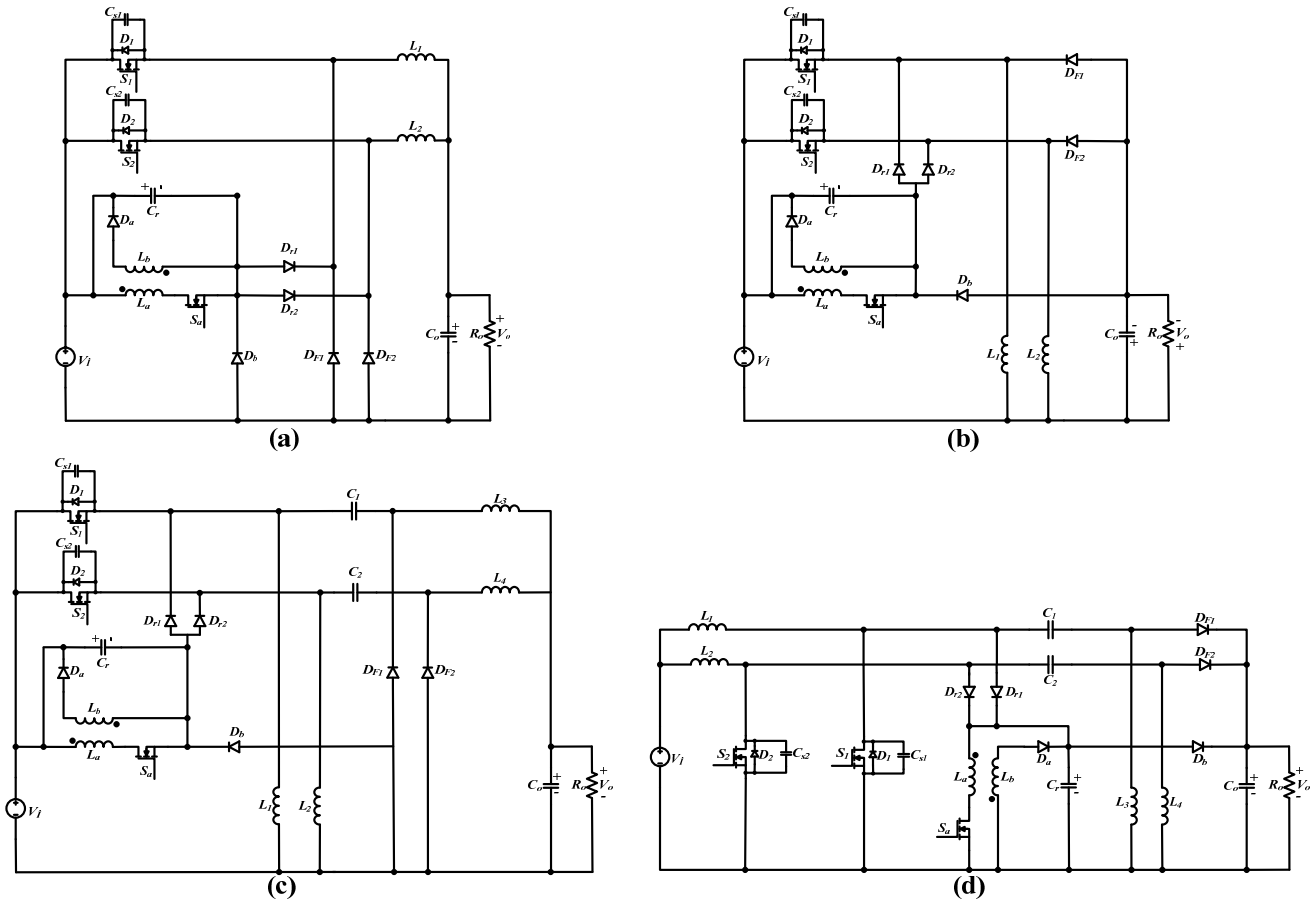


Fig. 8. Basic interleaved PWM converters with novel active snubber cell; (a) Interleaved Buck ZVT-PWM Converter, (b) Interleaved Buck-Boost ZVT-PWM Converter, (c) Interleaved Zeta ZVT-PWM Converter, (d) Interleaved Sepic ZVT-PWM Converter.

series inductor and turns off with ZVS because of the parallel capacitor.

3) The main diodes turn on with ZVS and turn off with ZCS. Therefore, their reverse recovery is eliminated.

4) No additional voltage or current stress is applied on the main switches and the main diodes.

5) All semiconductor devices turn on and off with soft switching techniques.

6) The switching power losses of all semiconductor devices are eliminated because of the soft switching techniques.

7) The conduction losses in the snubber cell are very low because the sum of the transient intervals is insignificant in the switching cycle.

8) The proposed converter can be operated even under light-load conditions.

9) The converter operates with soft switching in a wide duty cycle range.

10) With the interleaved approach, the ripples of the output voltage and input current are minimized.

11) This converter reduces the current stresses of the main devices because of its interleaved structure.

12) This converter reduces cost and size because soft switching is achieved by only one auxiliary switch, unlike some of the converters proposed in the literature.

13) The control of the converter is quite simple because the source terminals of the three switches are connected to a common point. In addition, this case resolves isolation problems, unlike some of the converters proposed in the literature.

14) Owing to the modular active snubber cell, this converter can be easily applied to other interleaved PWM converter topologies, as shown in Fig. 8.

V. Experimental Results

The experimental circuit of the proposed novel ZVT-PWM DC–DC interleaved boost converter is provided in Fig. 9. The proposed converter was implemented for the output voltage of 400 V and two input voltages, namely, 100 V and 250 V, at 500 W output power and 50 kHz switching frequency. A photograph of the experimental circuit is provided in Fig. 10. In the experimental prototype, the value of the output capacitor was 470 μF, the values of the main inductors were 1 mH, and the values of the resonant coupled inductors were 12 μH. The value of the resonant capacitor was 3.3 nF, and

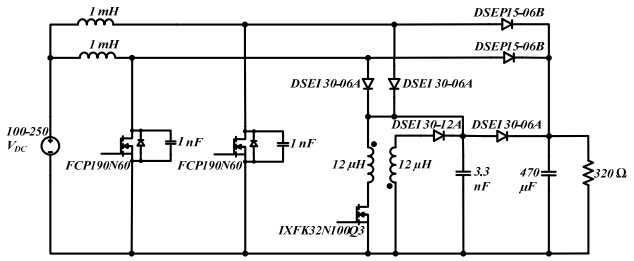


Fig. 9. Experimental circuit scheme of the proposed ZVT-PWM DC–DC interleaved boost converter.

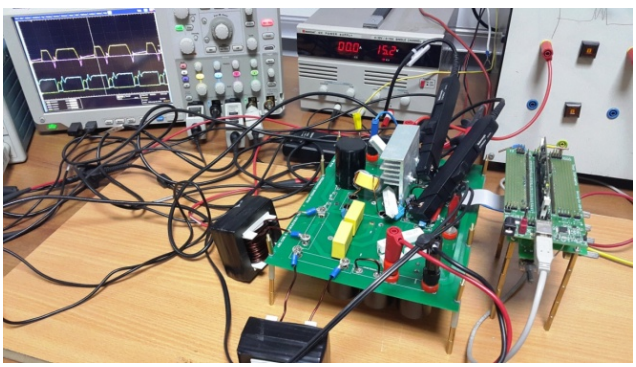


Fig. 10. Experimental circuit

TABLE IV
PART NUMBER AND NOMINAL VALUES OF THE SEMICONDUCTORS USED IN THE EXPERIMENTAL CIRCUIT

Device	Part Number	V (V)	I (A)	t_r (ns)	t_f (ns)	t_{rr} (ns)
S_1, S_2	FCP190N60	600	20.2	10	5	320
S_a	IXFK32N100Q3	1000	32	15	12	300
D_{F1}, D_{F2}	DSEP15-06B	600	15	-	-	25
D_{r1}, D_{r2}, D_b	DSEI 30-06A	600	37	-	-	35
D_a	DSEI 30-12A	600	26	-	-	40

the values of capacitors C_{s1} and C_{s2} were 1 nF. FCP190N60 switches ere used as the main switches, and the IXFK32N100Q3 switch was used as the auxiliary switch. In addition, DSEP15-06B diodes were used as the main diodes, as shown in Fig. 9.

In this study, the PWM control signals were obtained with code programmer CCS. Subsequently, these codes were loaded to a digital signal processor (DSP). Therefore, the control signals were obtained from the DSP. An analog-digital converter (ADC) was included in the DSP hardware to change the duty cycle of the control signals. The duty cycles of the control signals were adjusted optionally. In this study, the part number of the micro-processor used was DSP-TMS320F28335.

In the experimental circuit, normal Silicon diodes were used as the main and the auxiliary diodes. The part numbers and several major nominal values of the semiconductor devices used in the proposed converter are provided in Table IV, with reference to the datasheets of the manufacturers.

Fig. 11 shows the experimental results of the proposed ZVT-PWM DC–DC interleaved boost converter when the input voltage was 100 V and the output voltage was 400 V at a nominal power of 500 W. These results verified the theoretical analyses mentioned in the D > 50% mode. Fig. 11 (a) shows the control signals of auxiliary switch S_a and main switch S_1 and the voltage and current of S_1. As shown in the figure, the control signal was applied to the main switch when the current value of the main switch is negative. Therefore, the main switch turned on exactly with ZVT and turned off with ZVS. In addition, the main switch passed the boost inductor current, and the maximum voltage across the main switch was equal to the output voltage. Thus, no additional current or voltage stress was applied on the main switch. In addition, the figure shows that the control signal of the auxiliary switch was applied before 1.8 µs from the main switch.

Fig. 11 (b) shows the control signals of auxiliary switch S_a and main switch S_1 and the voltage and current of S_a. As seen in the figure, the auxiliary switch turned on with ZCS because of the series resonant inductor and turned off with ZVS because of the parallel resonant capacitor. In addition, the voltage across the auxiliary switch decreased through the RCD snubber that absorbed the energy of leakage inductance.

Fig. 11 (c) shows that main diode D_{F1} turned on with ZVS and turned off with ZCS. The reverse recovery losses of the main diode were eliminated because the main diode turned off with ZCS because of the series inductor. Moreover, no additional current or voltage stress was applied on the main diode.

Fig. 11 (d) shows the current of inductors L_a and L_b and the voltage of capacitor C_r. As shown in the figure, the energy of the snubber was transferred to the output after the voltage of C_r reached the output voltage.

Fig. 12 shows the experimental results of the proposed converter when the input voltage was 250 V and the output voltage was 400 V at a nominal power of 500 W. These results verified the theoretical analyses mentioned in the D < 50% mode.

Fig. 12 (a) shows that a control signal was applied to the auxiliary switch before 2.2 µs from the main switch. In addition, the main switch turned on exactly with ZVT and turned off with ZVS. Furthermore, no additional current and voltage stress was applied on the main switch in operating the D < 50 % mode. In Fig. 12 (b), the auxiliary switch turned on with ZCS and turned off with ZVS. Fig. 12 (c) shows that no additional current or voltage stress was applied on the main diode, and the main diode D_{F1} turned on with ZVS and turned off with ZCS. Therefore, the reverse recovery losses of the main diode were eliminated. Fig. 12 (d) shows that the energy of snubber was transferred to the output after the voltage of C_r reached the output voltage.

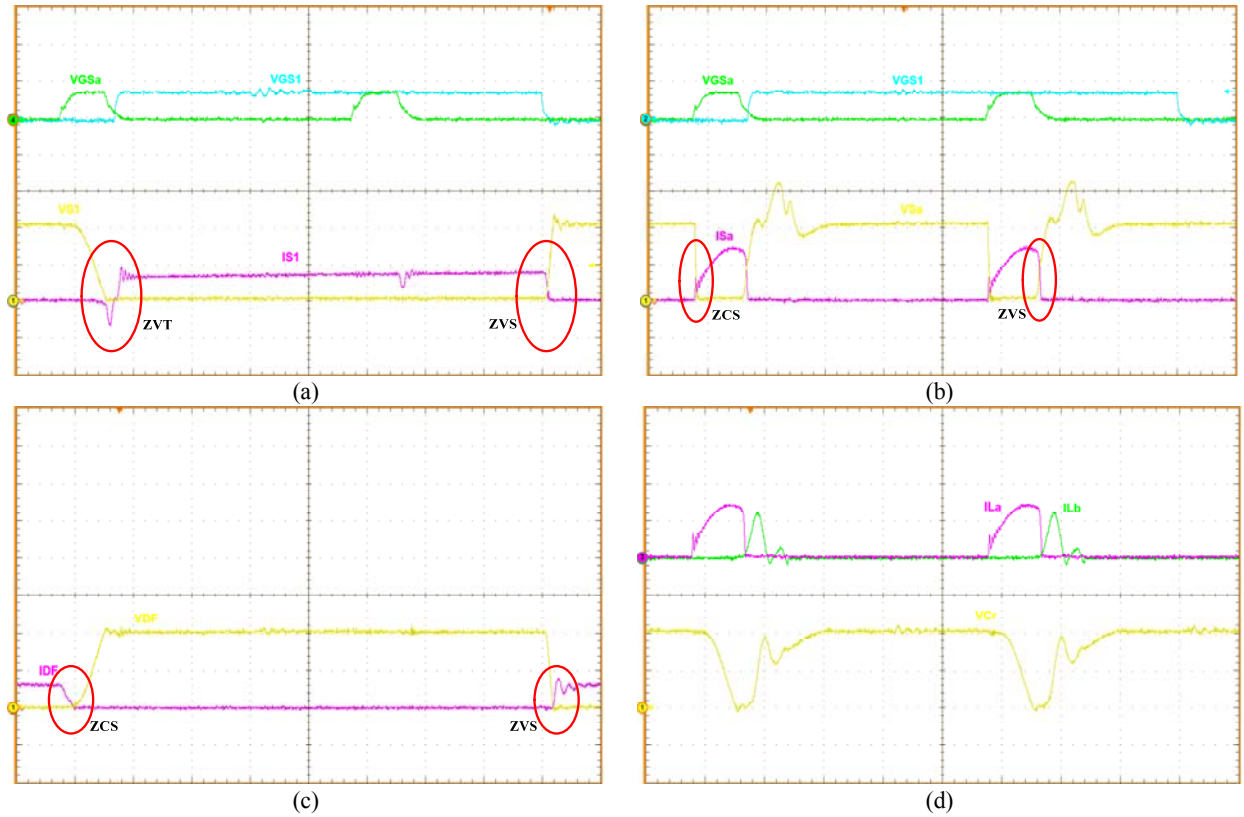


Fig. 11. Experimental results for D > 50% mode at 500 W; (a) Control signals of S_1, S_a and voltages and currents of S_1; (b) Control signals of S_1, S_a and voltage and current of S_a; (c) Voltage and current of D_F; (d) Current of inductors L_a and L_b and voltage of capacitor C_r (Voltage scale is 200V/div, current scale is 5A/div, control signal scale is 20V/div, and time scale is 2 μs/div).

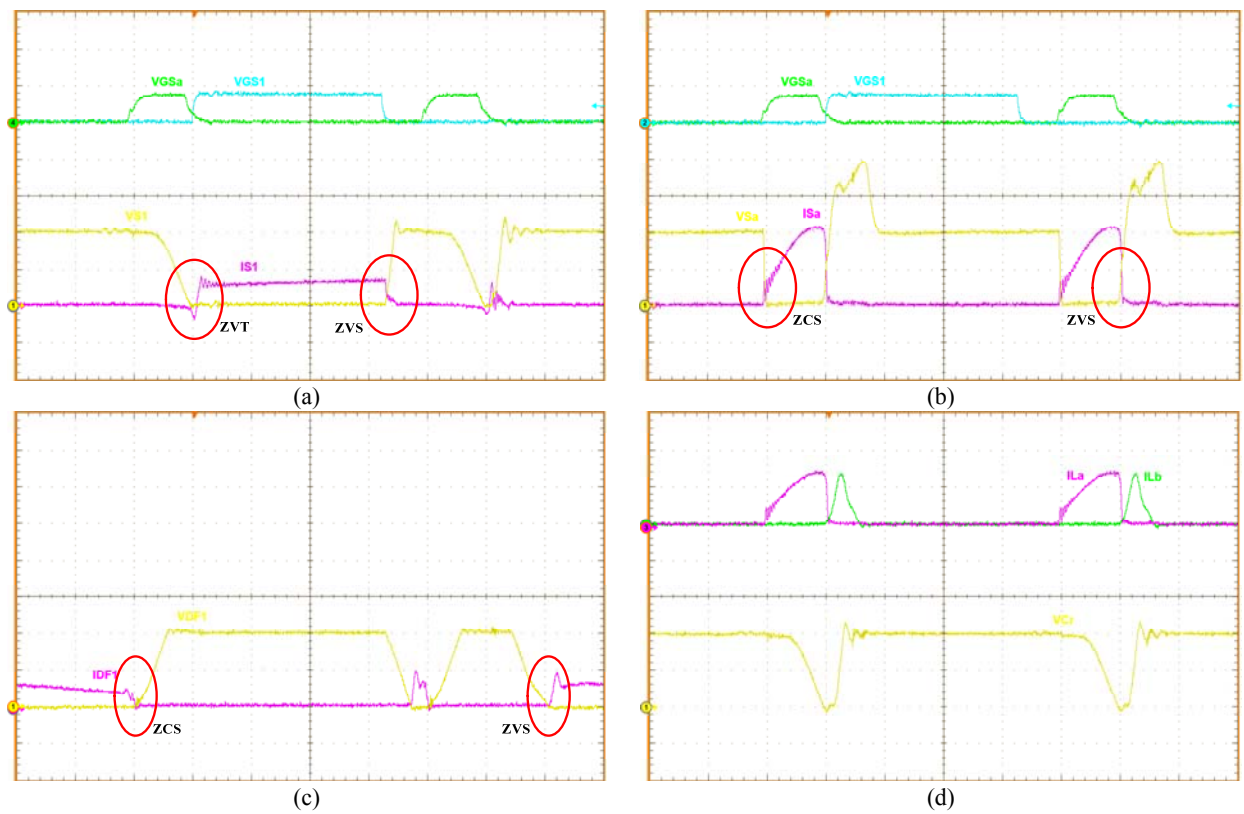
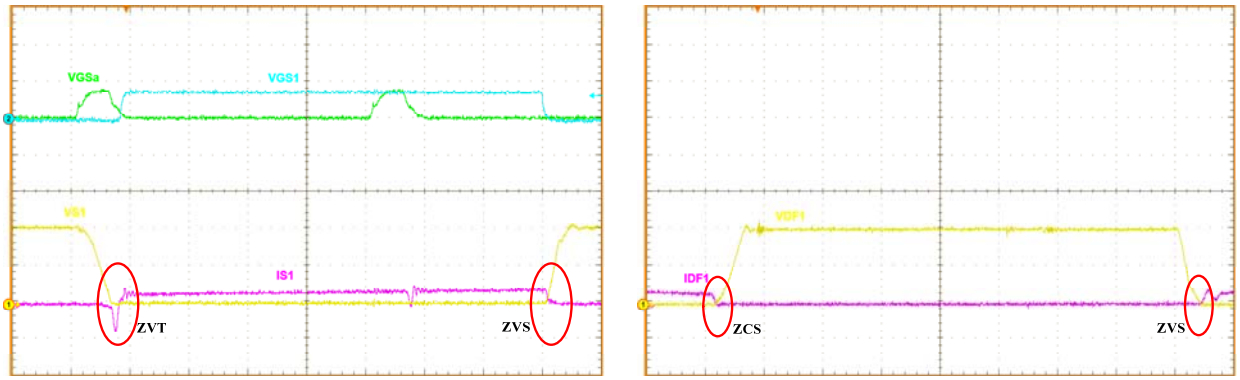


Fig. 12. Experimental results for the D < 50% mode at 500 W; (a) Control signals of S_1, S_a and voltages and currents of S_1; (b) Control signals of S_1, S_a and voltage and current of S_a; (c) Voltage and current of D_F; (d) and current of inductors L_a and L_b and voltage of capacitor C_r (Voltage scale is 200V/div, current scale is 2A/div, control signal scale is 20V/div, and time scale is 2 μs/div).



(a) (b)

Fig. 13. Experimental results for the D > 50% mode at 200 W; (a) Control signals of S_1, S_a and voltages and currents of S_1; (b) Voltage and current of D_F. (Voltage scale is 200V/div, current scale is 5A/div, control signal scale is 20V/div, and time scale is 2 μs/div).

TABLE V
SWITCHING OF DEVICES IN THE CONVERTER

Device	Turning on	Turning off
Main Switches S_1, S_2	ZVT	ZCT
Main Diodes D_{F1}, D_{F2}	ZVS	ZCS
Auxiliary Switch S_a	ZCS	ZVS
D_{r1}, D_{r2} Diodes	ZCS	ZVS
D_a , D_b Diodes	ZVS	ZCS

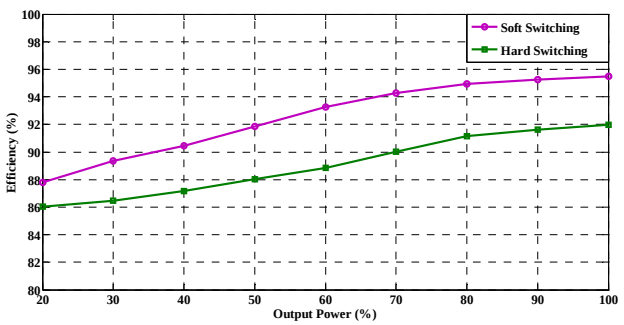


Fig. 14. Efficiency curves of the proposed converter in the case of SS and HS.

Consequently, all of the semiconductor devices turn on and off with SS. No additional current or voltage stress occurs on the main devices. The SS operation of the proposed converter is maintained for wide load ranges. Only the experimental results of switch S_1 and diode D_{F1} are provided here. Same results are valid for switch S_2 and diode D_{F2}. The results obtained by the switching of the semiconductor devices are provided in Table V.

The proposed converter also has an important advantage, such as operating at light loads. Fig. 13 shows the experimental results of the proposed converter when the input voltage is 100 V and the output voltage is 400 V at an output power of 200 W. As shown in the figure, the converter can achieve turning on and off with soft switching for semiconductor devices even under light-load conditions.

The target efficiency of the proposed converter is over 92% for the full load discussed in Section 3 design procedure. The efficiency of the proposed converter is examined for the operation with SS and HS. The efficiency curves are shown in Fig. 14, which shows that the efficiency values of the proposed converter are lower at low output power. The overall efficiency of the proposed converter, which is about 92% in HS, increases to about 95.5% because of SS at nominal output power. Converter loss is mainly caused by the circulating energy. The predicted operation principles and theoretical analysis of the proposed converter are verified with the experimental results.

VI. CONCLUSIONS

In this study, a novel ZVT-PWM DC–DC interleaved boost converter with an active snubber cell is proposed. The operating stages, key waveforms, design procedure, features, and experimental results of the proposed converter are provided in detail for the D > 50% and D < 50% modes. In this converter, the main switches turn on with ZVT and turn off with ZVS, and the main diodes turn on with ZVS and turn off with ZCS. The auxiliary switch turns on with ZCS and turns off with ZVS. In addition, the auxiliary diodes turn on and off with SS. Thus, the switching power losses in the classic interleaved boost converter are eliminated because of the proposed snubber cell. No extra conduction loss occurs because no additional voltage or current stress is applied on the main switches and diodes. The control of the converter is simple and low-cost because all switches are connected to the common ground and signal isolation is not required for the switches.

Through the interleaved approach, this converter minimizes the current stresses of the main devices and the ripple of the output voltage and input current. Therefore, the converter presents an attractive solution for high-power applications. Another important feature of the proposed converter is that the SS operation is maintained even under light load conditions. Finally, the overall efficiency of the classic interleaved boost converter of about 92% is increased to about 95.5% because of soft switching.

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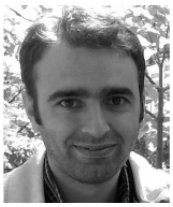
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